Dual 12-Bit (8-Bit Byte) Double-Buffered CMOS D/A Converter

DAC8248

FEATURES

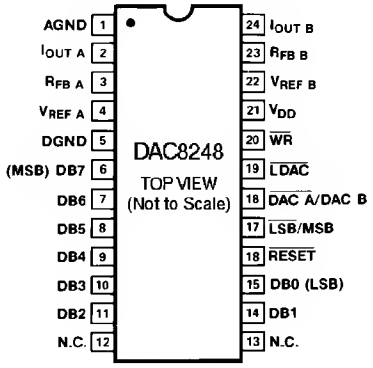
- Two Matched 12-Bit DACs on One Chip
- 12-Bit Resolution with an 8-Bit Data Bus
- Direct Interface with 8-Bit Microprocessors
- Double-Buffered Digital Inputs
- $\overline{\text{RESET}}$ to Zero Pin
- 12-Bit Endpoint Linearity (±1/2 LSB) Over Temperature
- +5 V to +15 V Single Supply Operation
- Latch-Up Resistant
- Improved ESD Resistance
- Packaged in a Narrow 0.3" 24-Pin DIP and 0.3" 24-Pin SOL Package
- Available in Die Form

APPLICATIONS

- Multichannel Microprocessor-Controlled Systems
- Robotics/Process Control/Automation
- Automatic Test Equipment
- Programmable Attenuator, Power Supplies, Window Comparators
- Instrumentation Equipment
- Battery Operated Equipment

PIN CONNECTIONS

24-Pin 0.3" Cerdip (W Suffix), 24-Pin Epoxy DIP (P Suffix), 24-Pin SOL (S Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

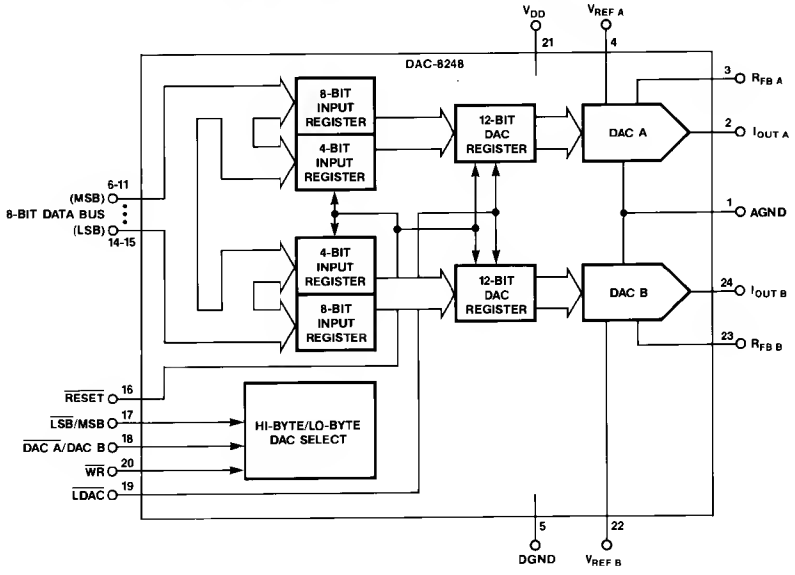
The DAC8248 is a dual 12-bit, double-buffered, CMOS digital-to-analog converter. It has an 8-bit wide input data port that interfaces directly with 8-bit microprocessors. It loads a 12-bit word in two bytes using a single control; it can accept either a least significant byte or most significant byte first. For designs with a 12-bit or 16-bit wide data path, choose the DAC8222 or DAC8221.

The DAC8248's double-buffered digital inputs allow both DAC's analog output to be updated simultaneously. This is particularly useful in multiple DAC systems where a common $\overline{\text{LDAC}}$ signal updates all DACs at the same time. A single $\overline{\text{RESET}}$ pin resets both outputs to zero.

The DAC8248's monolithic construction offers excellent DAC-to-DAC matching and tracking over the full operating temperature range. The DAC consists of two thin-film R-2R resistor ladder networks, two 12-bit, two 8-bit, and two 4-bit data registers, and control logic circuitry. Separate reference input and feedback resistors are provided for each DAC. The DAC8248

(continued on page 4)

FUNCTIONAL BLOCK DIAGRAM



REV. B

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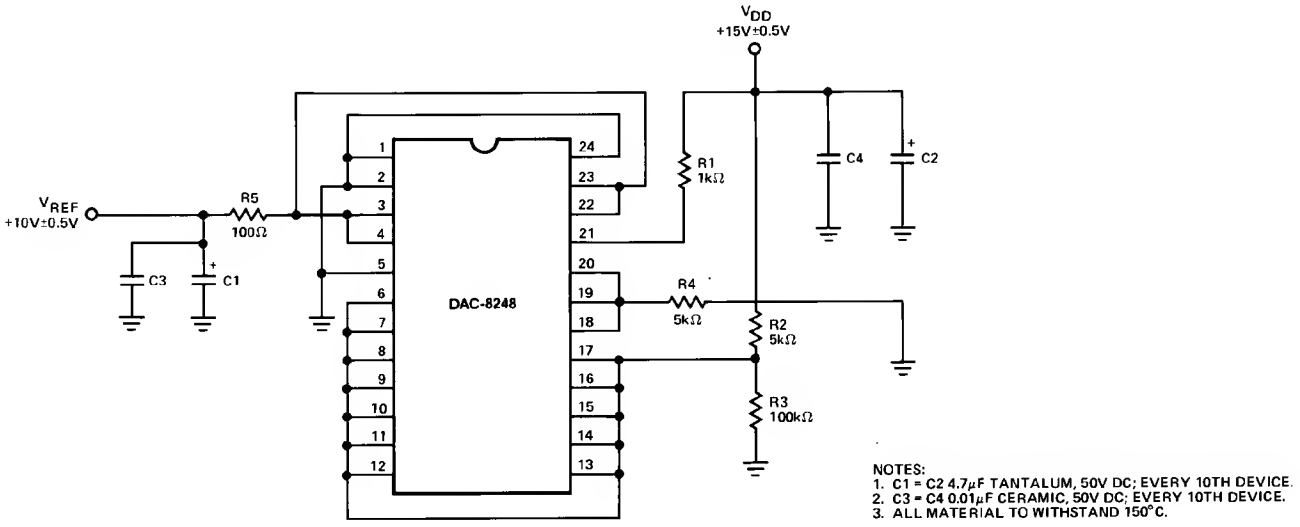
DAC8248–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{DD} = +5 V or +15 V; $V_{REF\,A}$ = $V_{REF\,B}$ = +10 V; V_{OUTA} = $V_{OUT\,B}$ = 0 V; AGND = DGND = 0 V; T_A = Full Temp Range specified in Absolute Maximum Ratings; unless otherwise noted. Specifications apply for DAC A and DAC B.)

Parameter	Symbol	Conditions	DAC8248 Min	Typ	Max	Units
STATIC ACCURACY						
Resolution	N		12			Bits
Relative Accuracy	INL	DAC8248A/E/G			±1/2	LSB
		DAC8248F/H			±1	LSB
Differential Nonlinearity	DNL	All Grades are Guaranteed Monotonic			±1	LSB
Full-Scale Gain Error[1]	G_{FSE}	DAC8248A/E			±1	LSB
		DAC8248G			±2	LSB
		DAC8248F/H			±4	LSB
Gain Temperature Coefficient (ΔGain/ΔTemperature)	TCG_{FS}	(Notes 2, 3) All Digital Inputs = 0s		±2	±5	ppm/°C
Output Leakage Current	I_{LKG}	T_A = +25°C		±5	±10	
$I_{OUT\,A}$ (Pin 2), $I_{OUT\,B}$ (Pin 24)		T_A = Full Temperature Range			±50	nA
Input Resistance ($V_{REF\,A,\,REF\,B}$)	R_{REF}	(Note 4)	8	11	15	kΩ
Input Resistance Match	$\frac{\Delta R_{REF}}{R_{REF}}$			±0.2	±1	%
DIGITAL INPUTS						
Digital Input High	V_{INH}	V_{DD} = +5 V	2.4			V
		V_{DD} = +15 V	13.5			V
Digital Input Low	V_{INL}	V_{DD} = +5 V			0.8	V
		V_{DD} = +15 V			1.5	V
Input Current (V_{IN} = 0 V		T_A = +25°C		±0.001	±1	µA
or V_{DD} and V_{INL} or V_{INH})	I_{IN}	T_A = Full Temperature Range			±10	µA
Input Capacitance	C_{IN}	DB0–DB11			10	pF
(Note 2)		$\overline{WR}$, $\overline{LDAC}$, $\overline{DAC\,A}$/DAC B, $\overline{LSB}$/MSB, $\overline{RESET}$			15	pF
POWER SUPPLY						
Supply Current	I_{DD}	Digital Inputs = V_{INL} or V_{INH}			2	mA
		Digital Inputs = 0 V or V_{DD}		10	100	µA
DC Power Supply Rejection Ratio (ΔGain/ΔV_{DD})	PSRR	ΔV_{DD} = ±5%			0.002	%/%
AC PERFORMANCE CHARACTERISTICS[2]						
Propagation Delay[5, 6]	t_{PD}	T_A = +25°C			350	ns
Output Current Setting Time[6, 7]	t_S	T_A = +25°C			1	µs
Output Capacitance	C_O	Digital Inputs = All 0s				
		$C_{OUT\,A}$, $C_{OUT\,B}$			90	pF
		Digital Inputs = All 1s				
		$C_{OUT\,A}$, $C_{OUT\,B}$			120	pF
AC Feedthrough at	FT_A	$V_{REF\,A}$ to $I_{OUT\,A}$; $V_{REF\,A}$ = 20 V p-p				
$I_{OUT\,A}$ or $I_{OUT\,B}$		f = 100 kHz; T_A = +25°C			–70	dB
	FT_B	$V_{REF\,B}$ to $I_{OUT\,B}$; $V_{REF\,B}$ = 20 V p-p				
		f = 100 kHz; T_A = +25°C			–70	dB

Parameter	Symbol	Conditions	DAC8248				Units
			V_{DD} = +5 V			V_{DD} = +15 V	
Switching Characteristics (Notes 2, 8)			+25°C	–40°C to +85°C (Note 9)	–55°C to +125°C	All Temps (Note 10)	
$\overline{LSB}$/MSB Select to Write Set-Up Time	t_{CBS}		130	170	180	80	ns min
$\overline{LSB}$/MSB Select to Write Hold Time	t_{CBH}		0	0	0	0	ns min
DAC Select to Write Set-Up Time	t_{AS}		180	210	220	80	ns min
DAC Select to Write Hold Time	t_{AH}		0	0	0	0	ns min
LDAC to Write Set-Up Time	t_{LS}		120	150	160	80	ns min
LDAC to Write Hold Time	t_{LH}		0	0	0	0	ns min
Data Valid to Write Set-Up Time	t_{DS}		160	210	220	70	ns min
Data Valid to Write Hold Time	t_{DH}		0	0	0	10	ns min
Write Pulse Width	t_{WR}		130	150	170	90	ns min
LDAC Pulse Width	t_{LWD}		100	110	130	60	ns min
Reset Pulse Width	t_{RWD}		80	90	90	60	ns min

NOTES
[1]Measured using internal $R_{FB\,A}$ and $R_{FB\,B}$. Both DAC digital inputs = 1111 1111 1111.
[2]Guaranteed and not tested.
[3]Gain TC is measured from +25°C to T_{MIN} or from +25°C to T_{MAX}.
[4]Absolute Temperature Coefficient is approximately +50 ppm/°C.
[5]From 50% of digital input to 90% of final analog output current. $V_{REF\,A} = V_{REF\,B}$ = +10 V; OUT A, OUT B load = 100 Ω, C_{EXT} = 13 pF.
[6]$\overline{WR}$, $\overline{LDAC}$ = 0 V; DB0–DB7 = 0 V to V_{DD} or V_{DD} to 0 V.
[7]Settling time is measured from 50% of the digital input change to where the output settles within 1/2 LSB of full scale.
[8]See Timing Diagram.
[9]These limits apply for the commercial and industrial grade products.
[10]These limits also apply as typical values for V_{DD} = +12 V with +5 V CMOS logic levels and T_A = +25°C.
Specifications subject to change without notice.



Burn-In Circuit

(continued from page 1)

operates on a single supply from +5 V to +15 V, and it dissipates less than 0.5 mW at +5 V (using zero or V_{DD} logic levels). The device is packaged in a space-saving 0.3", 24-pin DIP.

The DAC8248 is manufactured with PMI's highly stable thin-film resistors on an advanced oxide-isolated, silicon-gate, CMOS technology. PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted.)

V_{DD} to AGND ..... 0 V, +17 V
V_{DD} to DGND ..... 0 V, +17 V
AGND to DGND ..... –0.3 V, V_{DD} +0.3 V
Digital Input Voltage to DGND ..... –0.3 V, V_{DD} +0.3 V
$I_{OUT\,A}$, $I_{OUT\,B}$ to AGND ..... –0.3 V, V_{DD} +0.3 V
$V_{REF\,A}$, $V_{REF\,B}$ to AGND .....±25 V
$V_{RFB\,A}$, $V_{RFB\,B}$ to AGND .....±25 V
Operating Temperature Range
  AW Version .....–55°C to +125°C
  EW, FW, FP Versions .....–40°C to +85°C
  GP, HP, HS Versions .....0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature .....–65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

Package Type	θ_{JA}[1]	θ_{JC}	Units
24-Pin Hermetic DIP (W)	69	10	°C/W
24-Pin Plastic DIP (P)	62	32	°C/W
24-Pin SOL (S)	72	24	°C/W

NOTE
[1]θ_{JA} specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip and P-DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOL package.

CAUTION

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{FB}.
2. The digital control inputs are Zener-protected; however, permanent damage may occur on unprotected units from high energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Do not insert this device into powered sockets; remove power before insertion or removal.
4. Use proper antistatic handling procedures.
5. Devices can suffer permanent damage and/or reliability degradation if stressed above the limits listed under Absolute Maximum Ratings for extended periods. This is a stress rating only and functional operation at or above this specification is not implied.

ORDERING GUIDE[1]

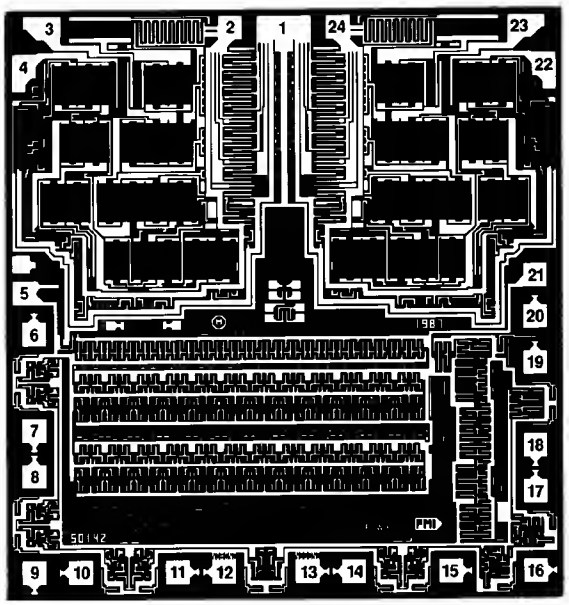
Model	Relative Accuracy (+5 V or +15 V)	Gain Error (+5 V or +15 V)	Temperature Range	Package Description
DAC8248AW[2]	±1/2 LSB	±1 LSB	–55°C to +125°C	24-Pin Cerdip
DAC8248EW	±1/2 LSB	±1 LSB	–40°C to +85°C	24-Pin Cerdip
DAC8248GP	±1/2 LSB	±2 LSB	0°C to +70°C	24-Pin Plastic DIP
DAC8248FW	±1 LSB	±4 LSB	–40°C to +85°C	24-Pin Cerdip
DAC8248HP	±1 LSB	±4 LSB	0°C to +70°C	24-Pin Plastic DIP
DAC8248FP	±1 LSB	±4 LSB	–40°C to +85°C	24-Pin Plastic DIP
DAC8248HS[3]	±1 LSB	±4 LSB	0°C to +70°C	24-Pin SOL

NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic DIP, and TO-can packages.
[2]For devices processed in total compliance to MIL-STD-883, add/883 after part number. Consult factory for 883 data sheet.
[3]For availability and burn-in information on SO and PLCC packages, contact your local sales office.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the DAC8248 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DICE CHARACTERISTICS



Die Size 0.124 × 0.132 inch, 16,368 sq. mils
(3.15 × 3.55 mm, 10.56 sq. mm)

1. AGND
2. I_{OUTA}
3. $R_{FB\ A}$
4. $V_{REF\ A}$
5. DGND
6. DB7(MSB)
7. DB6
8. DB5
9. DB4
10. DB3
11. DB2
12. NC
13. NC
14. DB1
15. DB0(LSB)
16. $\overline{RESET}$
17. $\overline{LSB}/MSB$
18. $\overline{DAC\ A}/DAC\ B$
19. $\overline{LDAC}$
20. $\overline{WR}$
21. V_{DD}
22. $V_{REF\ B}$
23. $R_{FB\ B}$
24. $I_{OUT\ B}$

SUBSTRATE (DIE BACKSIDE) IS INTERNALLY CONNECTED TO V_{DD}.

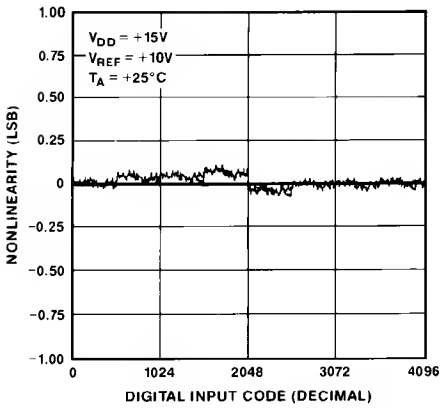
WAFER TEST LIMITS @ V_{DD} = +5 V or +15 V, $V_{REF\ A} = V_{REF\ B}$ = +10 V, $V_{OUT\ A} = V_{OUT\ B}$ = 0 V; AGND = DGND = 0 V; T_A = 25°C.

Parameter	Symbol	Conditions	DAC8248G Limit	Units
Relative Accuracy	INL	Endpoint Linearity Error	±1	LSB max
Differential Nonlinearity	DNL	All Grades are Guaranteed Monotonic	±1	LSB max
Full-Scale Gain Error[1]	G_{FSE}	Digital Inputs = 1111 1111 1111	±4	LSB max
Output Leakage ($I_{OUT\ A}$, $I_{OUT\ B}$)	I_{LKG}	Digital Inputs = 0000 0000 0000 Pads 2 and 24	±50	nA max
Input Resistance ($V_{REF\ A}$, $V_{REF\ B}$)	R_{REF}	Pads 4 and 22	8/15	kΩ min/kΩ max
$V_{REF\ A}$, $V_{REF\ B}$ Input Resistance Match	$\frac{\Delta R_{REF}}{R_{REF}}$		±1	% max
Digital Input High	V_{INH}	V_{DD} = +5 V	2.4	V min
		V_{DD} = +15 V	13.5	V min
Digital Input Low	V_{INL}	V_{DD} = +5 V	0.8	V max
		V_{DD} = +15 V	1.5	V max
Digital Input Current	I_{IN}	V_{IN} = 0 V or V_{DD}; V_{INL} or V_{INH}	±1	μA max
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH}	2	mA max
		All Digital Inputs 0 V or V_{DD}	0.1	mA max
DC Supply Rejection (ΔGain/ΔV_{DD})	PSR	ΔV_{DD} = ±5%	0.002	%/% max

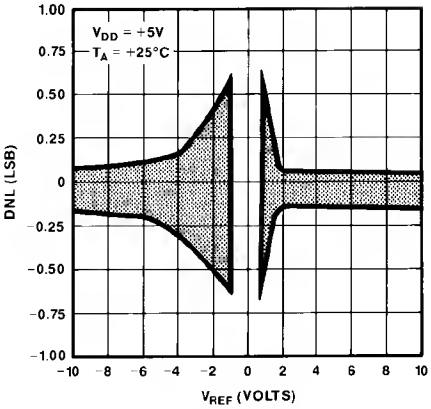
NOTES
[1]Measured using internal $R_{FB\ A}$ and $R_{FB\ B}$.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

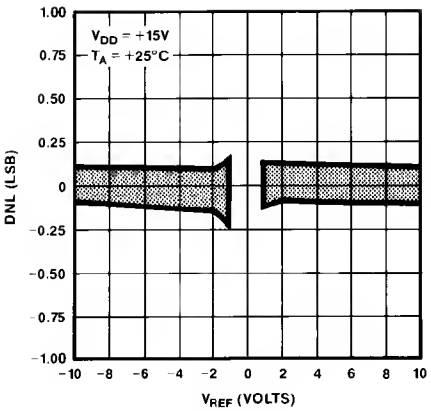
DAC8248- Typical Performance Characteristics



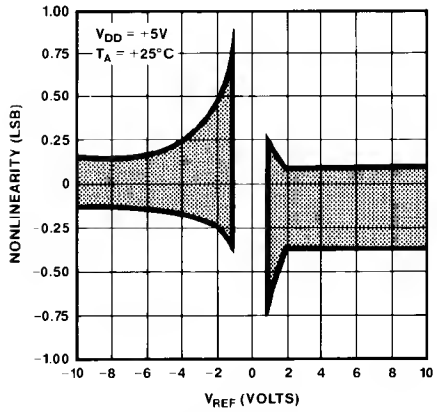
Channel-to-Channel Matching (DAC A & B are Superimposed)



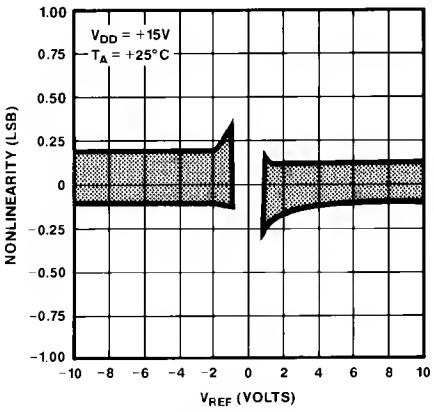
Differential Nonlinearity vs. V_{REF}



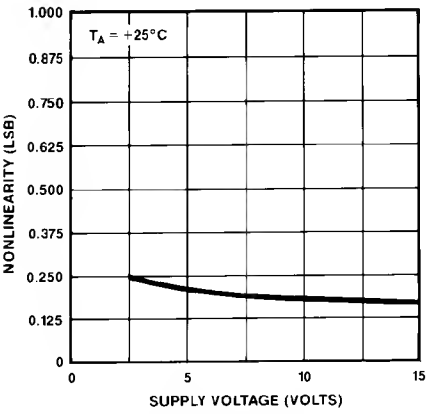
Differential Nonlinearity vs. V_{REF}



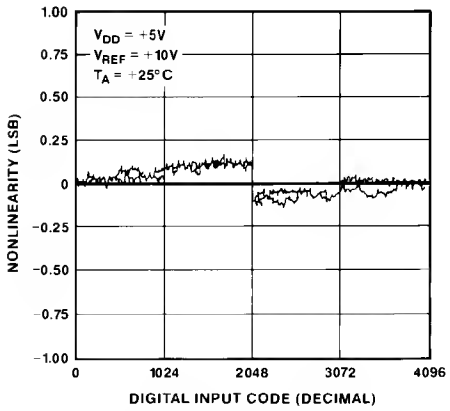
Nonlinearity vs. V_{REF}



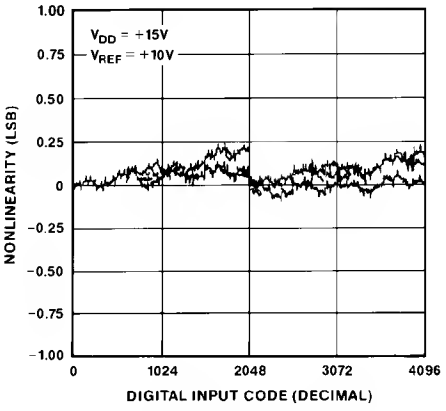
Nonlinearity vs. V_{REF}



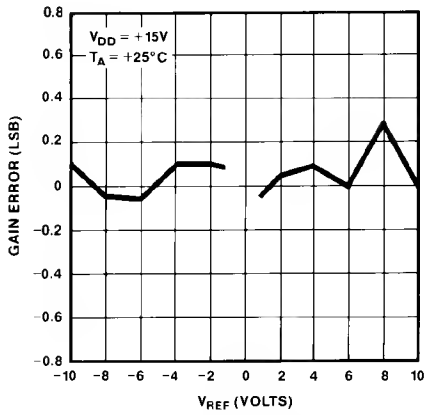
Nonlinearity vs. V_{DD}



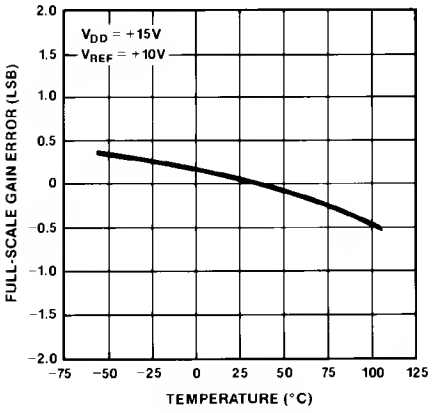
Nonlinearity vs. Code (DAC A & B are Superimposed)



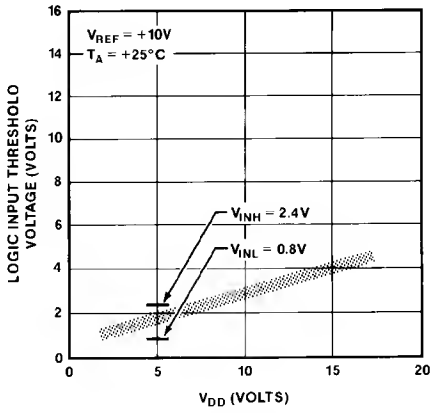
Nonlinearity vs. Code at T_A = –55°C, +25°C, +125°C for DAC A & B (All Superimposed)



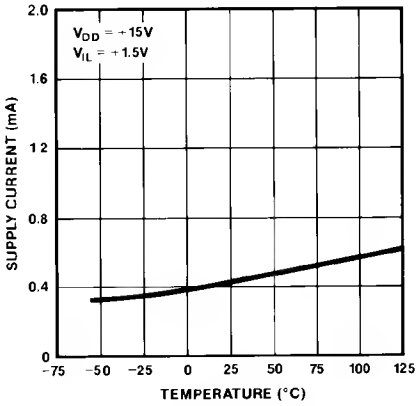
Absolute Gain Error Change vs. V_{REF}



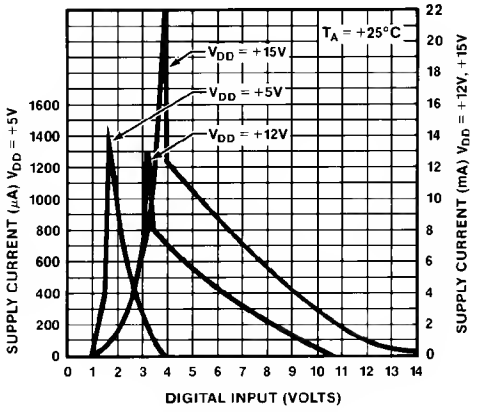
Full-Scale Gain Error vs. Temperature



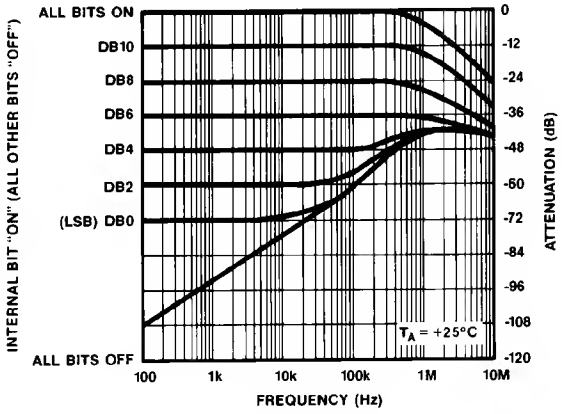
Logic Input Threshold Voltage vs. Supply Voltage (V_{DD})



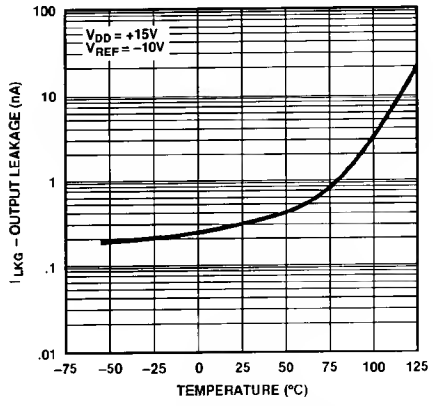
Supply Current vs. Temperature



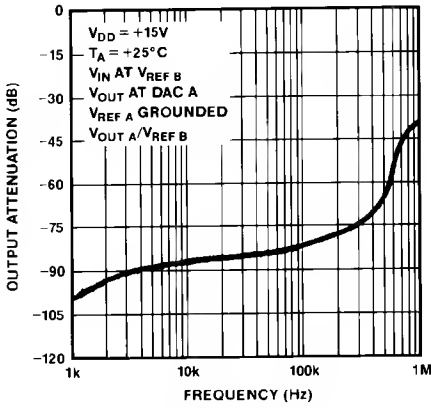
Supply Current vs. Logic Input Voltage



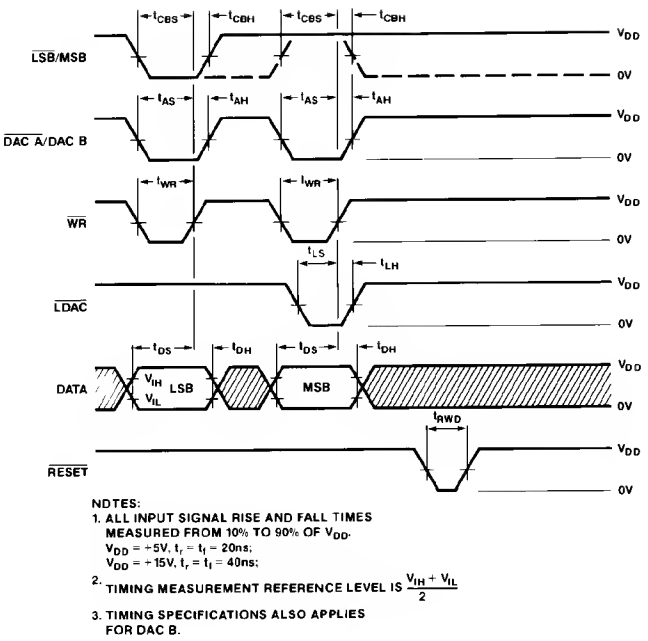
Multiplying Mode Frequency Response vs. Digital Code



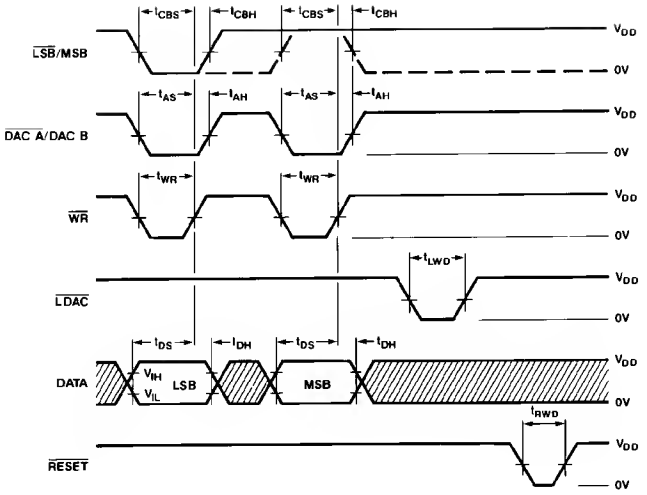
Output Leakage Current vs. Temperature



Analog Crosstalk vs. Frequency



Four Cycle Update



Five Cycle Update

Write Timing Cycle Diagram

PARAMETER DEFINITIONS

RESOLUTION (N)

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into; where n is equal to the number of bits.

RELATIVE ACCURACY (INL)

Relative accuracy, or integral nonlinearity, is the maximum deviation of the analog output (from the ideal) from a straight line drawn between the end points. It is expressed in terms of least significant bit (LSB), or as a percent of full scale.

DIFFERENTIAL NONLINEARITY (DNL)

Differential nonlinearity is the worst case deviation of any adjacent analog output from the ideal 1 LSB step size. The deviation of the actual "step size" from the ideal step size of 1 LSB is called the differential nonlinearity error or DNL. DACs with DNL greater than ±1 LSB may be nonmonotonic. ±1/2 LSB INL guarantees monotonicity and ±1 LSB maximum DNL.

GAIN ERROR (G_{FSE})

Gain error is the difference between the actual and the ideal analog output range, expressed as a percent of full-scale or in terms of LSB value. It is the deviation in slope of the DAC transfer characteristic from ideal.

Refer to PMI 1990/91 Data Book, Section 11, for additional digital-to-analog converter definitions.

GENERAL CIRCUIT DESCRIPTION

CONVERTER SECTION

The DAC8248 incorporates two multiplying 12-bit current output CMOS digital-to-analog converters on one monolithic chip. It contains two highly stable thin-film R-2R resistor ladder networks, two 12-bit DAC registers, two 8-bit input registers, and two 4-bit input registers. It also contains the DAC control logic circuitry and 24 single-pole, double-throw NMOS transistor current switches.

Figure 1 shows a simplified circuit for the R-2R ladder and transistor switches for a single DAC. R is typically 11 kΩ. The transistor switches are binarily scaled in size to maintain a constant voltage drop across each switch. Figure 2 shows a single NMOS transistor switch.

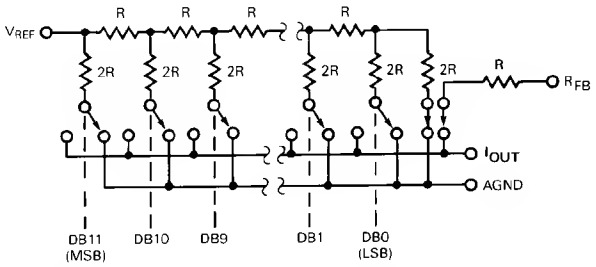


Figure 1. Simplified Single DAC Circuit Configuration. (Switches Are Shown For All Digital Inputs at Zero)

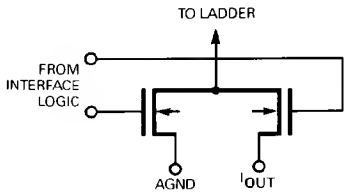


Figure 2. N-Channel Current Steering Switch

The binary-weighted currents are switched between I_{OUT} and AGND by the transistor switches. Selection between I_{OUT} and AGND is determined by the digital input code. It is important to keep the voltage difference between I_{OUT} and AGND terminals as close to zero as practical to preserve data sheet limits. It is easily accomplished by connecting the DAC's AGND to the noninverting input of an operational amplifier and I_{OUT} to the inverting input. The amplifier's feedback resistor can be eliminated by connecting the op amp's output directly to the DAC's R_{FB} terminal (by using the DAC's internal feedback resistor, R_{FB}). The amplifier also provides the current-to-voltage conversion for the DAC's output current.

The output voltage is dependent on the DAC's digital input code and V_{REF}, and is given by:

$$V_{OUT} = V_{REF} \times D/4096$$

where D is the digital input code integer number that is between 0 and 4095.

The DAC's input resistance, R_{REF}, is always equal to a constant value, R. This means that V_{REF} can be driven by a reference voltage or current, ac or dc (positive or negative). It is recommended that a low temperature-coefficient external R_{FB} resistor be used if a current source is employed.

The DAC's output capacitance (C_{OUT}) is code dependent and varies from 90 pF (all digital inputs low) to 120 pF (all digital inputs high).

To ensure accuracy over the full operating temperature range, permanently turned "ON" MOS transistor switches were included in series with the feedback resistor (R_{FB}) and the R-2R ladder's terminating resistor (see Figure 1). The gates of these NMOS transistors are internally connected to V_{DD} and will be turned "OFF" (open) if V_{DD} is not applied. If an op amp is using the DAC's R_{FB} resistor to close its feedback loop, then V_{DD} must be applied before or at the same time as the op amp's supply; this will prevent the op amp's output from becoming "open circuited" and swinging to either rail. In addition, some applications require the DAC's ladder resistance to fall within a certain range and are measured at incoming inspection; V_{DD} must be applied before these measurements can be made.

DIGITAL SECTION

The DAC8248's digital inputs are TTL compatible at V_{DD} = +5 V and CMOS compatible at V_{DD} = +15 V. They were designed to convert TTL and CMOS input logic levels into voltage levels that will drive the internal circuitry. The DAC8248 can use +5 V CMOS logic levels with V_{DD} = +12 V; however, supply current will increase to approximately 5 mA–6 mA.

Figure 3 shows the DAC's digital input structure for one bit. This circuitry drives the DAC registers. Digital controls, ϕ and $\bar{\phi}$, shown are generated from the DAC's input control logic circuitry.

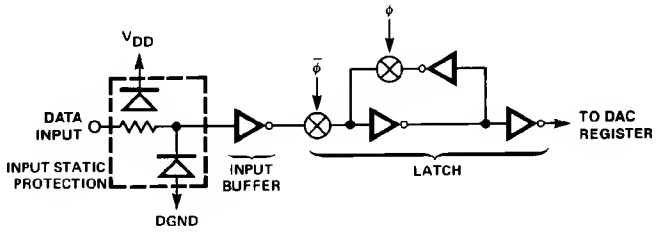


Figure 3. Digital Input Structure For One Bit

The digital inputs are electrostatic-discharge (ESD) protected with two internal distributed diodes as shown in Figure 3; they are connected between V_{DD} and DGND. Each input has a typical input current of less than 1 nA.

The digital inputs are CMOS inverters and draw supply current when operating in their linear region. Using a +5 V supply, the linear region is between +1.2 V to +2.8 V with current peaking at +1.8 V. Using a +15 V supply, the linear region is from +1.2 V to +12 V (current peaking at +3.9 V). It is recommended that the digital inputs be operated as close to the power supply voltage and DGND as is practically possible; this will keep supply currents to a minimum. The DAC8248 may be operated with any supply voltage between the range of +5 V to +15 V and still perform to data sheet limits.

The DAC8248's 8-bit wide data port loads a 12-bit word in two bytes: 8-bits then 4-bits (or 4-bits first then 8-bits, at users discretion) in a right justified data format. This data is loaded into the input registers with the $\overline{LSB}$/MSB and $\overline{WR}$ control pins.

Data transfer from the input registers to the DAC registers can be automatic. It can occur upon loading of the second data byte into the input register, or can occur at a later time through a strobed transfer using the $\overline{LDAC}$ control pin.

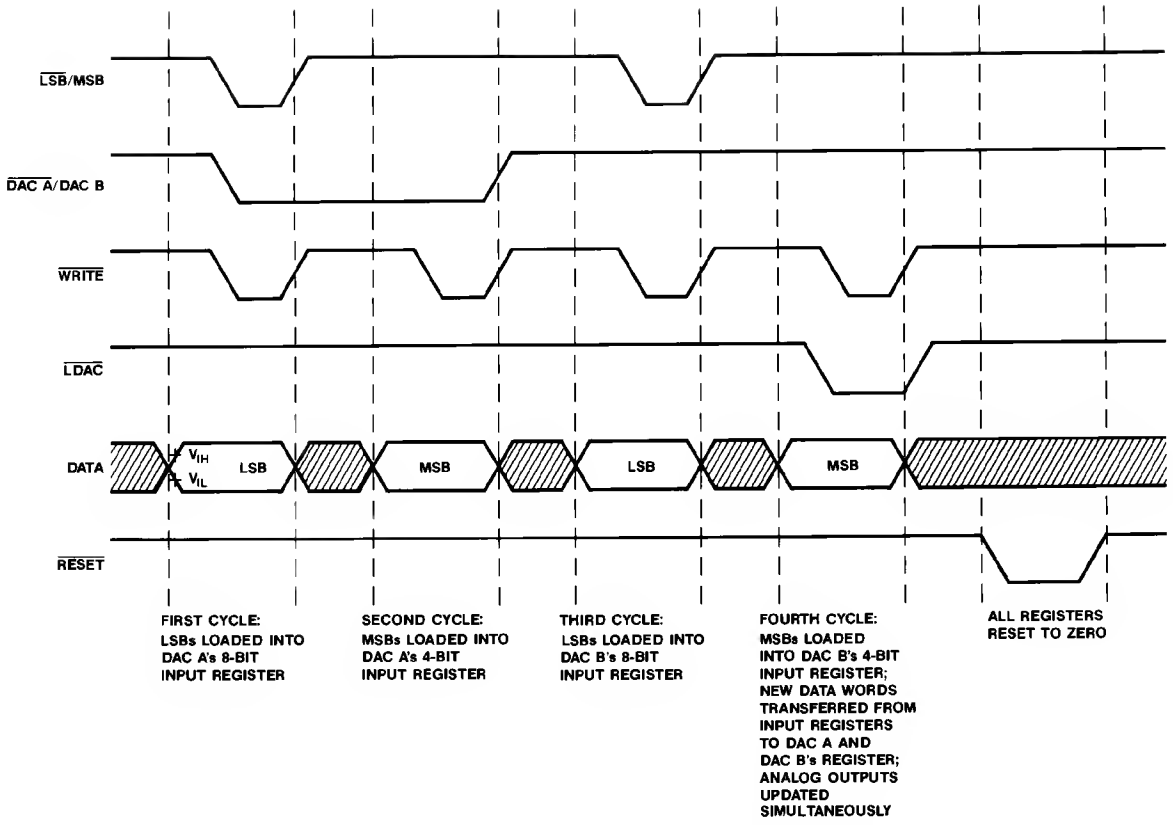


Figure 4. Four Cycle Update Timing Diagram

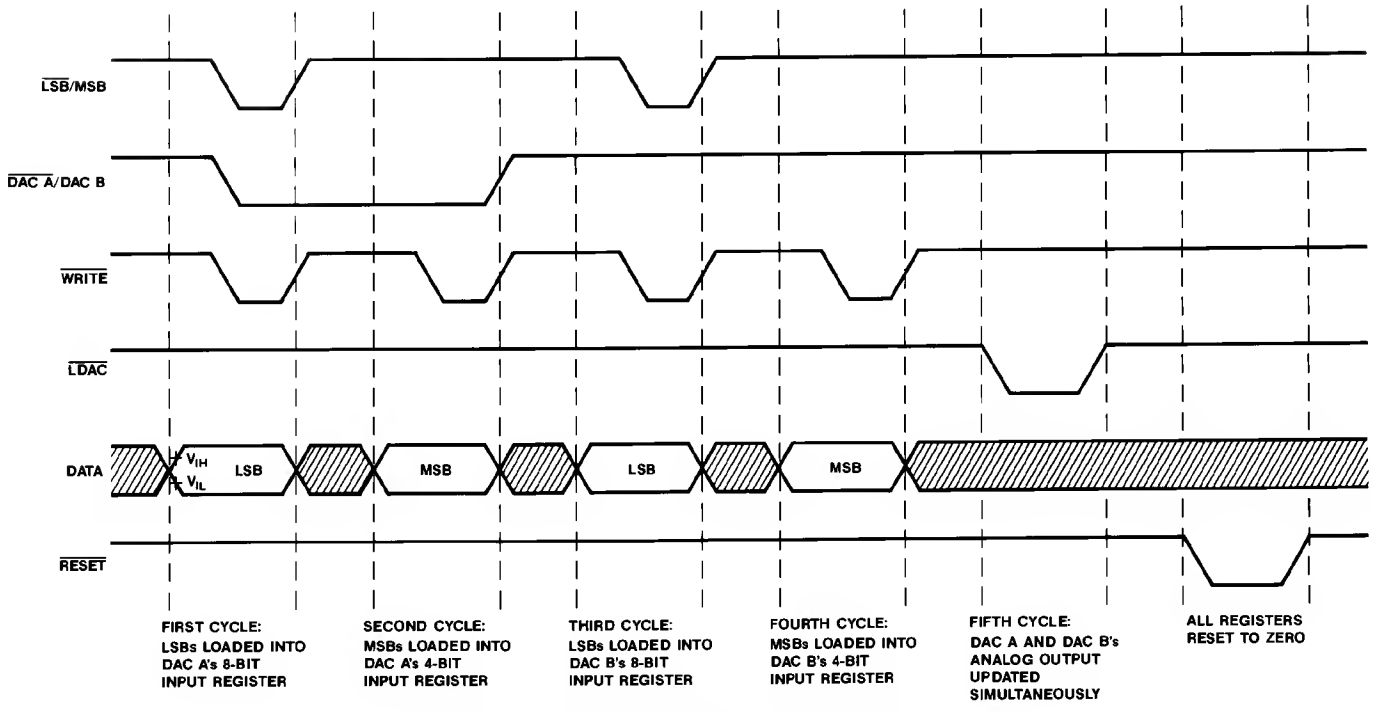


Figure 5. Five Cycle Update Timing Diagram

AUTOMATIC DATA TRANSFER MODE

Data may be transferred automatically from the input register to the DAC register. The first cycle loads the first data byte into the input register; the second cycle loads the second data byte and simultaneously transfers the full 12-bit data word to the DAC register. It takes four cycles to load and transfer two complete digital words for both DAC's, see Figure 4 (Four Cycle Update Timing Diagram) and the Mode Selection Table.

STROBED DATA TRANSFER MODE

Strobed data transfer allows the full 12-bit digital word to be loaded into the input registers and transferred to the DAC registers at a later time. This transfer mode requires five cycles: four to load two new data words into both DACs, and the fifth to transfer all data into the DAC registers. See Figure 5 (Five Cycle Update Timing Diagram) and the Mode Selection Table.

Strobed data transfer separating data loading and transfer operations serves two functions: the DAC output updating may be more precisely controlled, and multiple DACs in a multiple DAC system can be updated simultaneously.

RESET

The DAC8248 comes with a $\overline{\text{RESET}}$ pin that is useful in system calibration cycles and/or during system power-up. All registers are reset to zero when $\overline{\text{RESET}}$ is low, and latched at zero on the rising edge of the $\overline{\text{RESET}}$ signal when $\overline{\text{WRITE}}$ is high.

INTERFACE CONTROL LOGIC

The DAC8248's control logic is shown in Figure 6. This circuitry interfaces with the system bus and controls the DAC functions.

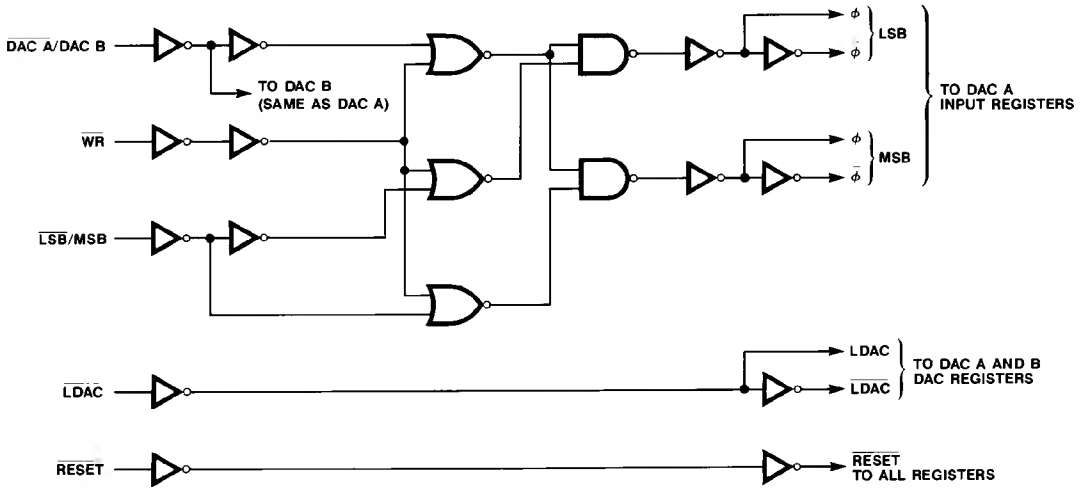


Figure 6. Input Control Logic

MODE SELECTION TABLE

DIGITAL INPUTS					REGISTER STATUS					
					DAC A			DAC B		
					Input Register		DAC	Input Register		DAC
$\overline{\text{DAC A/B}}$	$\overline{\text{WR}}$	$\overline{\text{LSB}}$/MSB	$\overline{\text{RESET}}$	$\overline{\text{LDAC}}$	LSB	MSB	Register	LSB	MSB	Register
L	L	L	H	H	WR	LAT	LAT	LAT	LAT	LAT
L	L	L	H	L	WR	LAT	WR	LAT	LAT	WR
L	L	H	H	H	LAT	WR	LAT	LAT	LAT	LAT
L	L	H	H	L	LAT	WR	WR	LAT	LAT	WR
H	L	L	H	H	LAT	LAT	LAT	WR	LAT	LAT
H	L	L	H	L	LAT	LAT	WR	WR	LAT	WR
H	L	H	H	H	LAT	LAT	LAT	LAT	WR	LAT
H	L	H	H	L	LAT	LAT	WR	LAT	WR	WR
X	H	X	H	H	LAT	LAT	LAT	LAT	LAT	LAT
X	H	X	H	L	LAT	LAT	WR	LAT	LAT	WR
X	X	X	L	X	ALL REGISTERS ARE RESET TO ZEROS					
X	H	X	↓	X	ZEROS ARE LATCHED IN ALL REGISTERS					

L = Low, H = High, X = Don't Care, WR = Registers Being Loaded, LAT = Registers Latched.

INTERFACE CONTROL LOGIC PIN FUNCTIONS

$\overline{\text{LSB}}$/MSB – (PIN 17) $\overline{\text{LEAST SIGNIFICANT BIT}}$ (Active Low)/ MOST SIGNIFICANT BIT (Active High). Selects lower 8-bits (LSBs) or upper 4-bits (MSBs); either can be loaded first. It is used with the $\overline{\text{WR}}$ signal to load data into the input registers. Data is loaded in a right justified format.

$\overline{\text{DAC A}}$/DAC B – (PIN 18) DAC SELECTION. Active low for DAC A and Active High for DAC B.

$\overline{\text{WR}}$ – (PIN 20) $\overline{\text{WRITE}}$ – Active Low. Used with the $\overline{\text{LSB}}$/MSB signal to load data into the input registers, or Active High to latch data into the input registers.

$\overline{\text{LDAC}}$ – (PIN 19) LOAD DAC. Used to transfer data simultaneously from DAC A and DAC B input registers to both DAC output registers. The DAC register becomes transparent (activity on the digital inputs appear at the analog output) when both $\overline{\text{WR}}$ and $\overline{\text{LDAC}}$ are low. Data is latched into the output registers on the rising edge of $\overline{\text{LDAC}}$.

$\overline{\text{RESET}}$ – (PIN 16) – Active Low. Functions as a zero override; all registers are forced to zero when the $\overline{\text{RESET}}$ signal is low. All registers are latched to zeros when the write signal is high and $\overline{\text{RESET}}$ goes high.

APPLICATIONS INFORMATION

UNIPOLAR OPERATION

Figure 7 shows a simple unipolar (2-quadrant multiplication) circuit using the DAC8248 and OP270 dual op amp (use two OP42s for applications requiring higher speeds), and Table I shows the corresponding code table. Resistors R1, R2, and R3, R4 are used only if full-scale gain adjustments are required.

Table I. Unipolar Binary Code Table (Refer to Figure 7)

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUT} (DAC A or DAC B)
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -\frac{1}{2}V_{REF}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0 V

NOTE

$1\ LSB = (2^{-12})\ (V_{REF}) = \frac{1}{4096}\ (V_{REF})$

Low temperature-coefficient (approximately 50 ppm/°C) resistors or trimmers should be used. Maximum full-scale error without these resistors for the top grade device and V_{REF} = ±10 V is 0.024%, and 0.049% for the low grade. Capacitors C1 and C2 provide phase compensation to reduce overshoot and ringing when high-speed op amps are used.

Full-scale adjustment is achieved by loading the appropriate DAC's digital inputs with 1111 1111 1111 and adjusting R1 (or R3 for DAC B) so that:

$$V_{OUT} = V_{REF} \times \left(\frac{4095}{4096}\right)$$

Full-scale can also be adjusted by varying V_{REF} voltage and eliminating R1, R2, R3, and R4. Zero adjustment is performed by

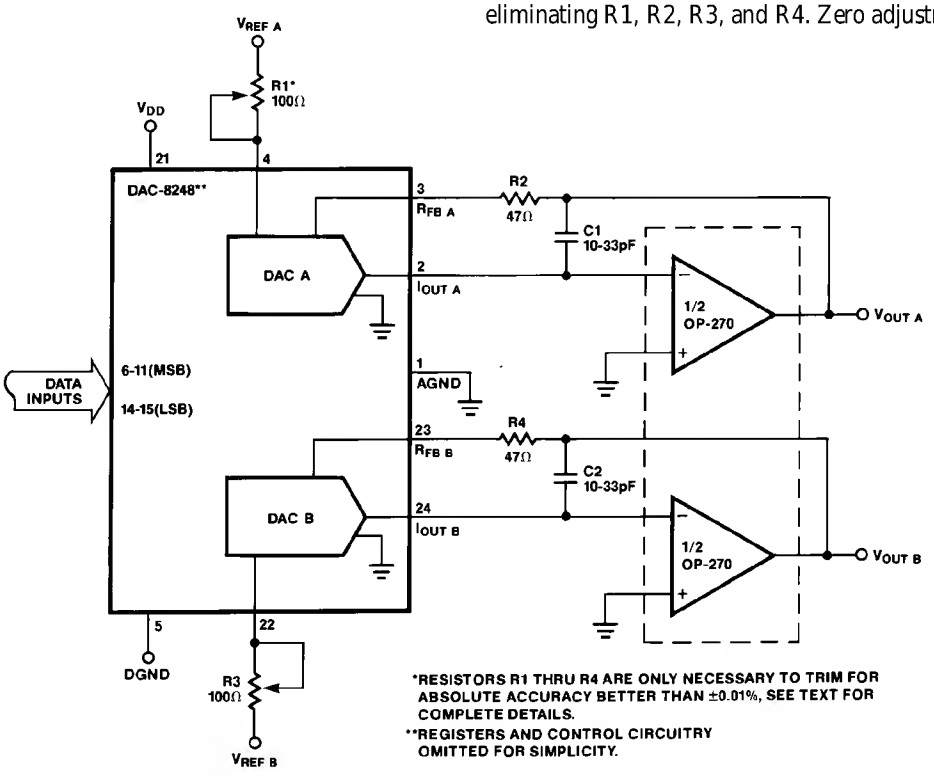


Figure 7. Unipolar Configuration (2-Ouadrant Multiplication)

loading the appropriate DAC's digital inputs with 0000 0000 0000 and adjusting the op amp's offset voltage to 0 V. It is recommended that the op amp offset voltage be adjusted to less than 10% of 1 LSB (244 μV), and over the operating temperature range of interest. This will ensure the DAC's monotonicity and minimize gain and linearity errors.

BIPOLAR OPERATION

The bipolar (offset binary) 4-quadrant configuration using the DAC8248 is shown in Figure 8, and the corresponding code is shown in Table II. The circuit makes use of the OP470, a quad op amp (use four OP42s for applications requiring higher speeds).

The full-scale output voltage may be adjusted by varying V_{REF} or the value of R5 and R8, and thus eliminating resistors R1, R2, R3, and R4. If resistors R1 through R4 are omitted, then R5, R6, R7 (R8, R9, and R10 for DAC B) should be ratio-matched to 0.01% to keep gain error within data sheet specifications. The resistors should have identical temperature-coefficients if operating over the full temperature range.

Zero and full-scale are adjusted in one of two ways and are at the users discretion. Zero-output is adjusted by loading the appropriate DAC's digital inputs with 1000 0000 0000 and varying R1 (R3 for DAC B) so that $V_{OUT\,A}$ (or $V_{OUT\,B}$) equals 0 V. If R1, R2 (R3, R4 for DAC B) are omitted, then zero output can be adjusted by varying R6, R7 ratios (R9, R10 for DAC B). Full-scale is adjusted by loading the appropriate DAC's digital inputs with 1111 1111 1111 and varying R5 (R8 for DAC B).

Table II. Bipolar (Offset Binary) Code Table (Refer to Figure 8)

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUT} (DAC A or DAC B)
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0 V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

NOTE:

$1\,LSB = (2^{-11})(V_{REF}) = \frac{1}{2048}(V_{REF})$

SINGLE SUPPLY OPERATION

CURRENT STEERING MODE

Because the DAC8248's R-2R resistor ladder terminating resistor is internally connected to AGND, it lends itself well for single supply operation in the current steering mode configuration. This means that AGND can be raised above system

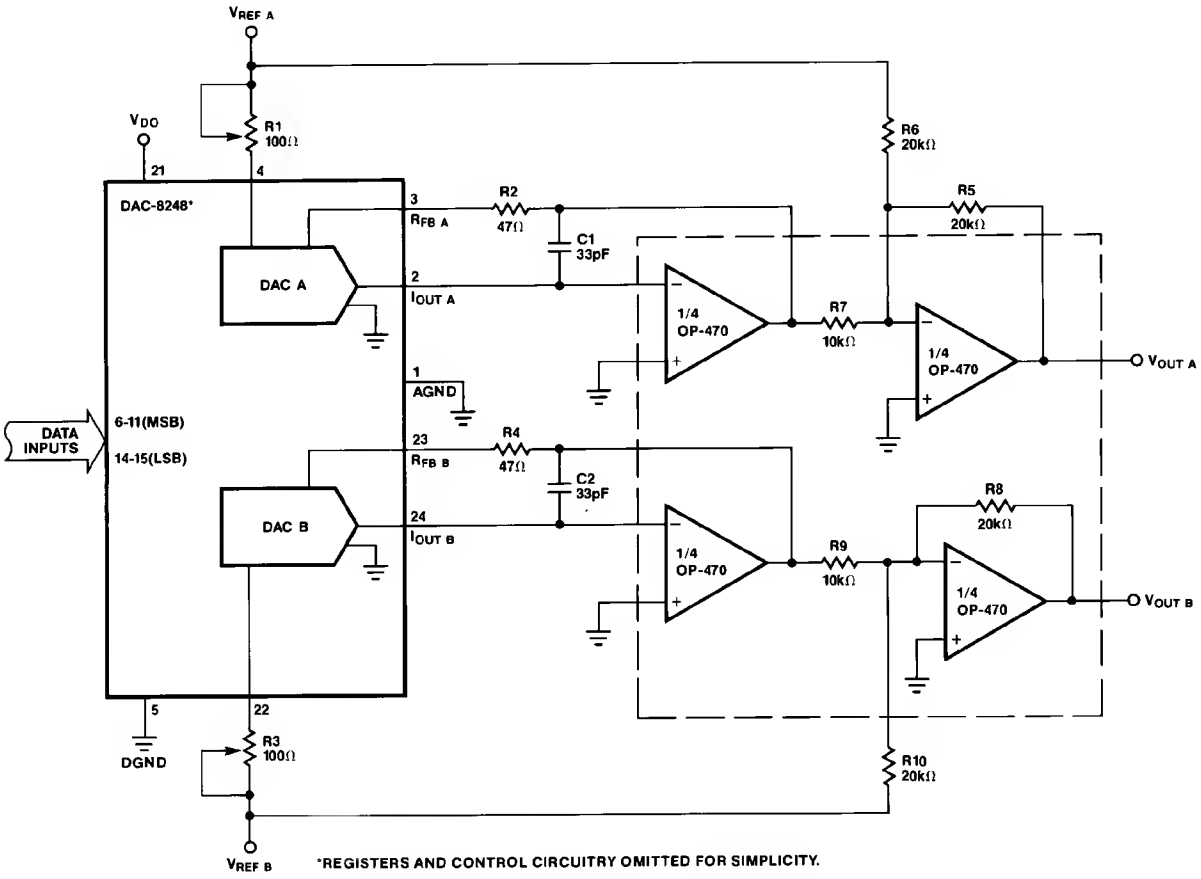


Figure 8. Bipolar Configuration (4-Quadrant Multiplication)

ground as shown in Figure 9. The output voltage will be between +5 V and +10 V depending on the digital input code. The output expression is given by:

$$V_{OUT} = V_{OS} \times (D/4096)(V_{OS})$$

where V_{OS} = Offset Reference Voltage (+5 V in Figure 9)

D = Decimal Equivalent of the Digital Input Word

VOLTAGE SWITCHING MODE

Figure 10 shows the DAC8248 in another single supply configuration. The R-2R ladder is used in the voltage switching mode and functions as a voltage divider. The output voltage (at the V_{REF} pin) exhibits a constant impedance R (typically 11 kΩ) and must be buffered by an op amp. The R_{FB} pins are not used and are left open. The reference input voltage must be maintained within +1.25 V of AGND, and V_{DD} between +12 V and +15 V; this ensures that device accuracy is preserved.

The output voltage expression is given by:

$$V_{OUT} = V_{REF} (D/4096)$$

where D = Decimal Equivalent of the Digital Input Word

APPLICATIONS TIPS

GENERAL GROUND MANAGEMENT

Grounding techniques should be tailored to each individual system. Ground loops should be avoided, and ground current paths should be as short as possible and have a low impedance.

The DAC8248's AGND and DGND pins should be tied together at the device socket to prevent digital transients from appearing at the analog output. This common point then becomes the single ground point connection. AGND and DGND is then brought out separately and tied to their respective power supply grounds. Ground loops can be created if both grounds are tied together at more than one location, i.e., tied together at the device and at the digital and analog power supplies.

PC board ground plane can be used for the single point ground connection should the connections not be practical at the device socket. If neither of these connections are practical or allowed, then the device should be placed as close as possible to the systems single point ground connection. Back-to-back Schottky diodes should then be connected between AGND and DGND.

POWER SUPPLY DECOUPLING

Power supplies used with the DAC8248 should be well filtered and regulated. Local supply decoupling consisting of a 1 μF to 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic is highly recommended. The capacitors should be connected between the V_{DD} and DGND pins and at the device socket.

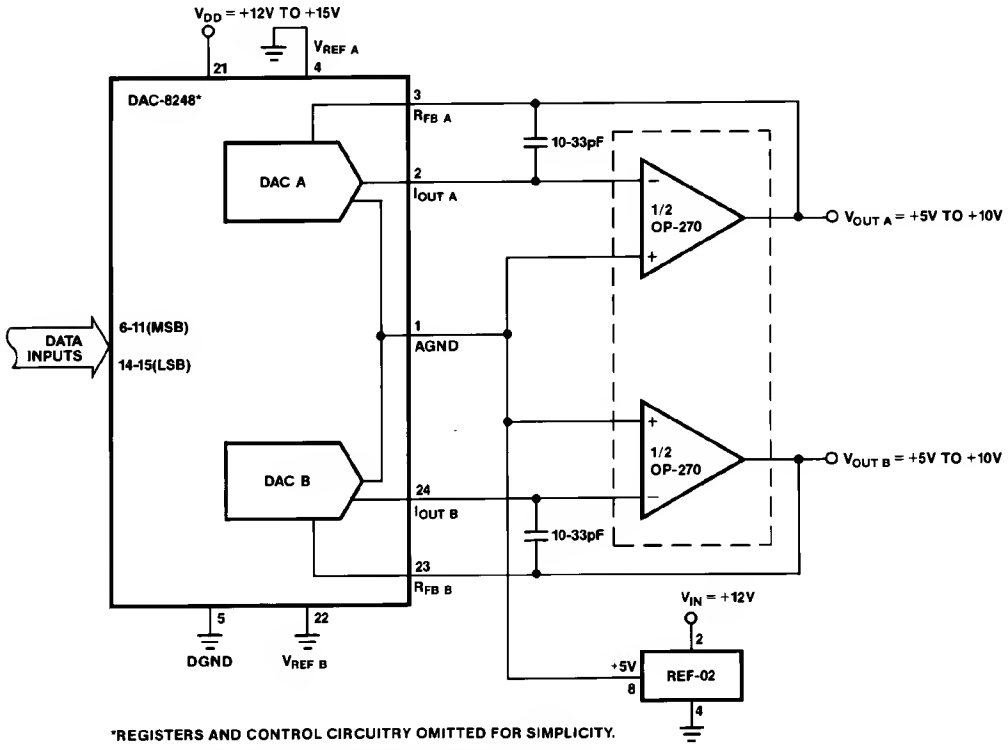
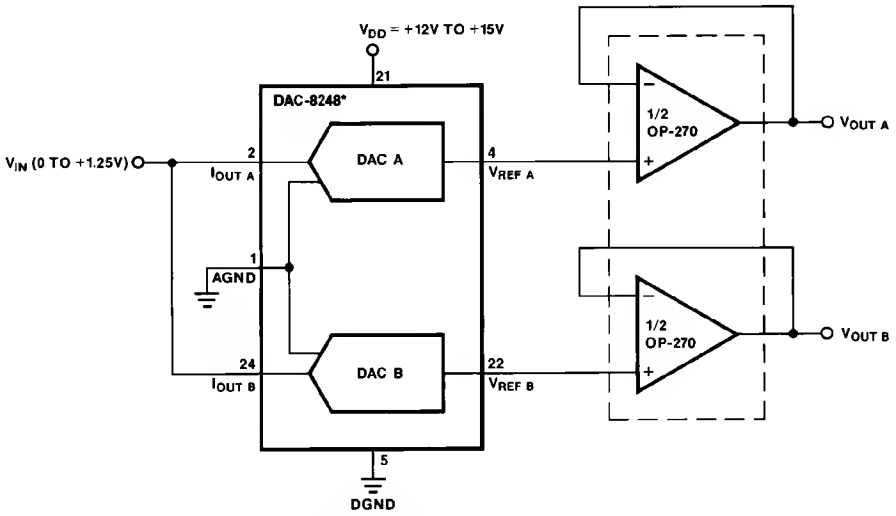
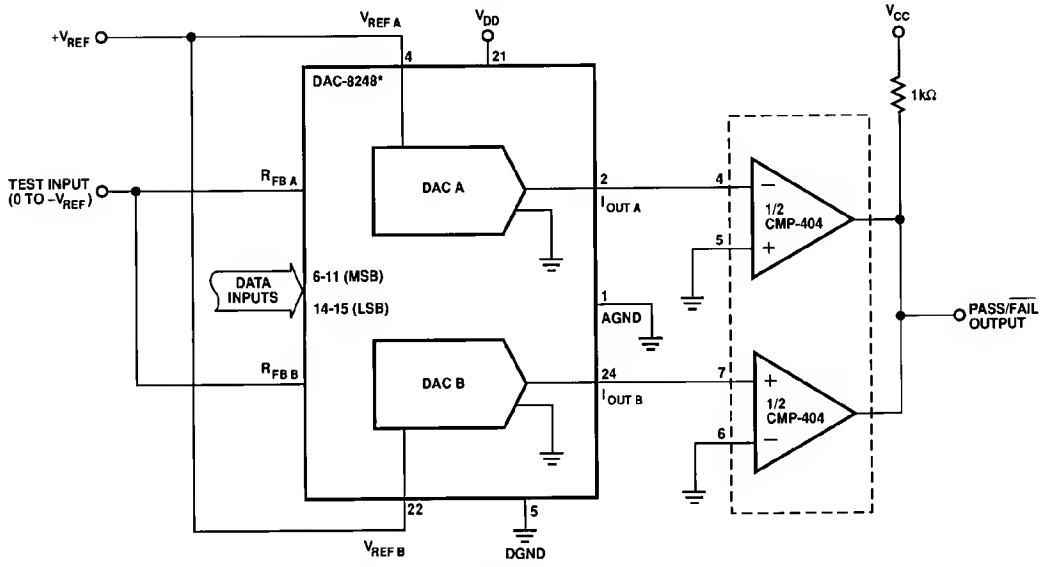


Figure 9. Single Supply Operation (Current Switching Mode)



*REGISTERS AND DIGITAL CIRCUITRY OMITTED FOR SIMPLICITY.

Figure 10. Single Supply Operation (Voltage Switching Mode)

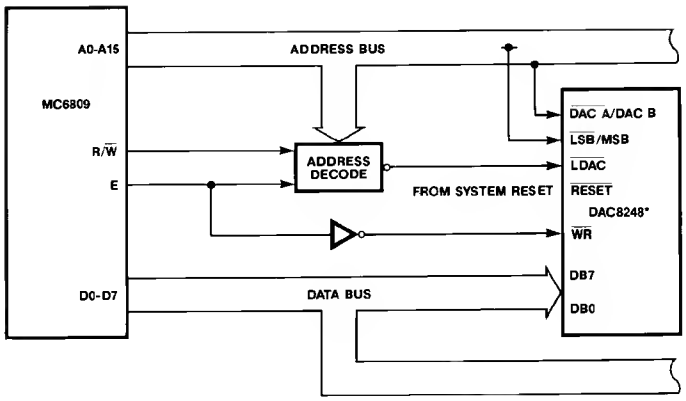


*REGISTERS AND CONTROL CIRCUITRY OMITTED FOR SIMPLICITY.

Figure 11. Digitally-Programmable Window Detector (Upper/Lower Limit Detector)

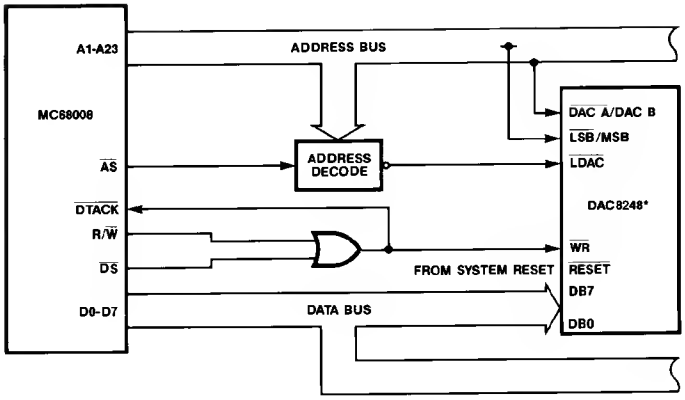
MICROPROCESSOR INTERFACE CIRCUITS

The DAC8248s versatile loading structure allows direct interface to an 8-bit microprocessor. Its simplicity reduces the number of required glue logic components. Figures 12 and 13 show the DAC8248 interface configurations with the MC6809 and MC68008 microprocessors.



*REGISTERS AND DIGITAL CIRCUITRY OMITTED FOR SIMPLICITY.

Figure 12. DAC8248 to MC6809 Interface



*REGISTERS AND CONTROL CIRCUITRY OMITTEO FOR SIMPLICITY.

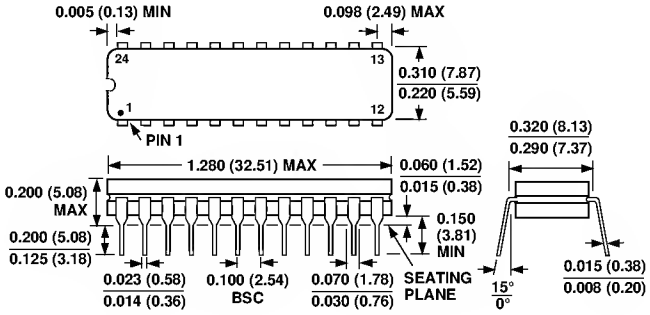
Figure 13. DAC8248 to MC68008 Interface

000000000

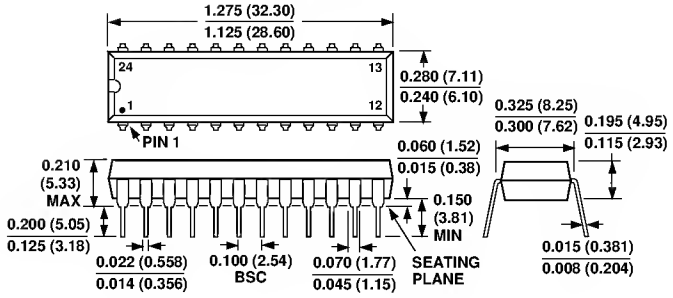
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

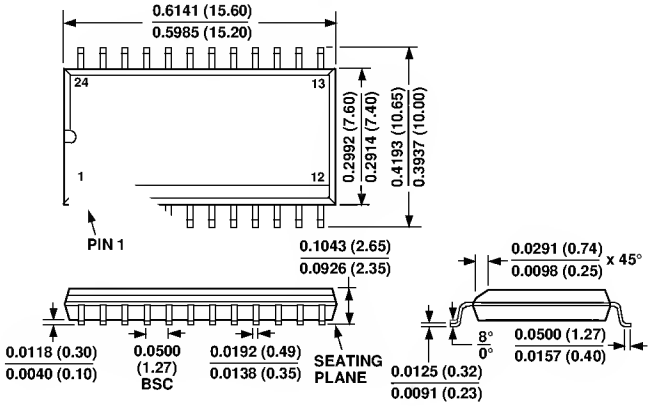
24-Lead Cerdip (Q-24)



24-Lead Plastic DIP (N-24)



24 Lead SOL (R-24)



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